

Message Text

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ORIGIN EB-07

INFO OCT-01 CIAE-00 COME-00 DODE-00 NRC-05 NSAE-00 USIA-06
TRSE-00 EUR-12 ERDA-05 ISO-00 /036 R

DRAFTED BY EB/ITP/EWT--LROSS:JAS
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RPE

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FM SECSTATE WASHDC
TO USMISSION OECD PARIS PRIORITY

C O N F I D E N T I A L STATE 305214

EXCON

E.O. 11652: XGDS-1

TAGS: ESTC, COCOM, HU, JA

SUBJECT: JAPANESE PROCESS CONTROL SYSTEM TO HUNGARY--
IL 1565

REF: A) COCOM DOC (76) 1432 AND CORRIGENDUM,
B) COCOM DOC (76) 1733

1. NO OBJECTION IN LIGHT OF SAFEGUARDS JAPANESE ARE APPLYING.
2. U.S. TECHNICIANS CONCUR IN THE CALCULATED PDR OF 16.85 MBITS PER SECOND, FOR A SINGLE CPU, BASED ON AVERAGE FLOATING-POINT EXECUTION TIMES AND A FIXED-POINT ADDITION TIME OF 2.63 MICROSECONDS FOR A 32-BIT INSTRUCTION. IN A SYSTEM WITH MULTIPLE CPU'S ACCESSING A GLOBAL MEMORY, SUCH AS THIS
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ONE, THEY TREAT THE PDR SIMILARLY TO THE CPU BUS RATE, AND THEREFORE, BY NOTE 16 (A) TO IL 1565, DERIVE AN OVERALL PDR OF 33.7 MBITS PER SECOND FOR THE PROCESS CONTROL SYSTEM.

3. BY NOTE 16 (N) THE TOTAL NUMBER OF ACCESSES IS BASED ON TWO PERIPHERAL MEMORY DEVICES WITH 10 MILLISECONDS AVERAGE

ACCESS TIME, PLUS THREE MEMORY DEVICES EACH HAVING 46 MILLI-
SECONDS AVERAGE ACCESS TIME, FOR A TOTAL OF 265.2 ACCESSES
PER SECOND FOR THE SYSTEM.
ROBINSON

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NNN

Message Attributes

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